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it is specified in section 3 1 7 clock synchronization in nxp i2c bus specification and user manual um10204 there shall be no difference in the flowchart of start signal between smbus and i2c main differences between i2c and smbus are explained in 4 2 smbus system management bus i nxp i2c bus specification document, **i2c data sampling is done at clock edge or level** - the i2c interface is a de facto standard that is now controlled by nxp search for the nxp i2c bus specification and user manual um10204 the standard specifies a data bit setup time before the rising edge of the clock and a data hold time after the falling edge of the clock so a receiver could potentially use either edge of the clock or could use a level sensitive latch when the clock is, **using feature set of i2c master on tm4c129x microcontrollers** - um10204 i2c bus specification and user manual 2 1 physical layer of i2c the i2c bus consists of two signals serial clock scl and serial data sda at the io level both scl and sda are open drain as shown in figure 1 figure 1 open drain circuit 2 using feature set of i2c master on tm4c129x microcontrollers spma073 july 2015, **i2c bus specification and user manual wordpress com** - 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